Design of Diamond Chips with a Spherical Architecture in Thorium-Powered Production Infrastructures as an Enhancement for High-Performance Computing

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Abstract

The semiconductor industry faces three converging crises: the end of Moore's Law, the unsustainable cooling requirements of high-performance chips, and the depletion of critical material supply chains. This article proposes a radical alternative for classical computing architecture that integrates four disruptive technologies: (1) a multilayer spherical substrate of synthetic polycrystalline diamond that maximises integration density and dissipates heat in three dimensions, (2) a hybrid acousto-optic lithography system that enables the patterning of three-dimensional interconnections on a curved surface, (3) copper interconnections using hybrid bonding with sub-10 µm pitch for ultra-high-density vertical links, and (4) a fourth-generation molten salt thorium reactor (MSR-TMSR) as a source of energy and process heat for industrial manufacturing. The proposed architecture offers thermal conductivity up to five times higher than copper (2000-2200 $W \cdot m^{-1} \cdot K^{-1}$), an estimated 60-80 % reduction in cooling energy consumption, and a net-negative carbon footprint through atmospheric carbon capture during diamond synthesis. Its applications in artificial intelligence data centres, high-performance computing (HPC) systems, and power electronics for extreme environments are analysed, along with a realistic technological roadmap based on existing prototypes of each subsystem.

Keywords: Synthetic diamond, spherical chips, acoustic lithography, 3D hybrid bonding, thorium salt reactor, high-performance computing, thermal management, energy sustainability.

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1. Introduction

1.1 The Triple Crisis of the Semiconductor Industry

The semiconductor industry, cornerstone of the digital economy, faces unprecedented challenges in the 2020s. First, Moore's Law — the observation that the number of transistors per chip doubles approximately every two years — has shown clear signs of deceleration. As transistors approach atomic scales of 2 nm and 3 nm, quantum effects, current leakage, and manufacturing variability impose physical barriers that are increasingly difficult to overcome with traditional planar architectures.

Second, the thermal management crisis has become the dominant bottleneck for high-performance computing (HPC) systems and artificial intelligence data centres. Current chips reach power densities exceeding 100 $W \cdot cm^{-2}$, and 2.5D and 3D chiplet architectures — which stack multiple dies in close proximity — pose even more extreme heat densities. Conventional thermal interface materials (TIMs) are reaching their limits, and direct liquid cooling, although effective, adds complexity and cost.

Third, the dependence on critical materials (silicon, germanium, indium, rare earths) and geopolitical tensions in supply chains have highlighted the vulnerability of the current semiconductor manufacturing model. The industry needs alternatives based on abundant, recyclable materials with low energy requirements.

1.2 Motivation and Objectives

Faced with this landscape, this article proposes a radical alternative that departs from established paradigms: instead of continuing to optimise planar silicon wafers, we propose to completely reimagine the chip architecture, the base material, and its energy source. The architecture presented here integrates emerging technologies that have already demonstrated their viability in the laboratory or in prototypes, although they have never been combined in the way proposed here. Our objective is to demonstrate, through theoretical analysis and references to the existing literature, that this synergistic integration could offer decisive advantages in integration density, thermal efficiency, and energy sustainability.

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2. Description of the Architecture

The proposed architecture consists of four interdependent technological pillars, the joint operation of which is illustrated in Figure 1.

Figure 1. Conceptual scheme of the proposed architecture. *(Diagrammatic representation)*

2.1 Multilayer Spherical Substrate of Synthetic Diamond

2.1.1 Synergistic Properties of Diamond as a Substrate

Synthetic polycrystalline diamond obtained by chemical vapour deposition (CVD) offers an unparalleled combination of properties for classical high-performance computing. Its thermal conductivity, the highest of any known material with values of 2000-2200 $W \cdot m^{-1} \cdot K^{-1}$, exceeds that of copper (about 400 $W \cdot m^{-1} \cdot K^{-1}$) by more than five times and that of silicon (about 150 $W \cdot m^{-1} \cdot K^{-1}$) by almost two orders of magnitude. This property allows the heat generated by millions of transistors to spread immediately throughout the entire volume of the substrate, eliminating the hot spots that limit the performance of silicon chips.

Furthermore, diamond is an ultra-wide-bandgap semiconductor with a bandgap of 5.5 eV, compared to 1.1 eV for silicon or 3.4 eV for silicon carbide. This allows it to withstand much higher breakdown voltages (up to 10 times higher than silicon) and to operate in temperature ranges that would render any other conventional semiconductor useless — from -200 °C to over 500 °C — without significant degradation.

2.1.2 The Geometric Advantage of the Sphere

The choice of a spherical geometry, instead of the conventional flat wafer, responds to considerations of volumetric integration, interconnection, and thermal dissipation. In a sphere, the heat generated by active circuits arranged in concentric layers is conducted radially towards the surface, following a spherical wavefront that rapidly reduces the heat density. Radial symmetry also minimises interconnection distances between layers, since the shortest path between two points in different layers is radial, with a maximum length equal to the sphere's radius.

From the integration point of view, a sphere of diameter D provides a surface approximately four times larger than a flat disk of the same diameter if concentric active layers are used (assuming a layer thickness $t << D$). This volumetric gain translates directly into greater computing capacity per unit of "footprint" on the motherboard.

2.1.3 Diamond-Thorium Symbiosis

Synthetic diamond manufacturing by CVD requires substrate temperatures of 700-900 °C and a constant supply of high-purity precursor gases (methane, hydrogen). These conditions align perfectly with the output profile of a thorium salt reactor, which typically operates at 600-700 °C at atmospheric pressure and can supply high-quality process heat directly without conversion to electricity. To date, CVD processes on curved surfaces have been developed for the manufacture of diamond capsules for inertial confinement fusion, demonstrating the feasibility of growing polycrystalline diamond on spherical substrates.

2.2 Hybrid Acousto-Optic Lithography for 3D Patterning

The manufacture of integrated circuits on a spherical surface presents unique challenges for which conventional photolithography is not prepared. The hybrid acousto-optic lithography we propose combines two complementary techniques.

First, acoustic lithography uses very high-frequency ultrasound waves (MHz to GHz) to model pressure fields that guide the deposition of materials (such as photoresists or metals) onto the spherical surface. Techniques such as holographic direct sound printing (HDSP) have demonstrated the ability to create precise three-dimensional patterns using acoustic holograms, and picosecond ultrasonics allows the characterisation of buried structures with line widths of up to 100 nm — a resolution that, while not reaching state-of-the-art transistors, is sufficient for medium-scale interconnections and passive layers.

Second, solid-state acousto-optic deflectors (AODs) allow laser writing beams to be directed with rapidity and no moving parts, combining the best of both technologies: the acoustic ability to pattern conformally on curved surfaces and the nanometric resolution of optical lithography for critical transistor levels. This hybrid approach enables the scalable and precise fabrication of spherical chips.

2.3 Interconnections Using 3D Hybrid Bonding

To connect the multiple active layers of the spherical chip to each other and provide I/O paths to the outside, the architecture employs copper hybrid bonding (Cu-Cu) technology, which is emerging as the industry standard for chiplet integration and advanced 3D packaging. This technology combines in a single process dielectric bonding (SiO_2 to SiO_2) with direct copper-to-copper bonding, eliminating conventional solder microbumps and achieving interconnection pitches below 10 µm. The advantages for our architecture are multiple:

- **Ultra-high connection density:** Hybrid bonding supports interconnection densities of the order of 10^5 to 10^6 connections per square millimetre, essential for communication between layers of a multilayer sphere.
- **Reduced resistance and latency:** By eliminating intermediate solders, the contact resistance per interconnection can be reduced by up to 90 % compared to traditional techniques, with a consequent improvement in the energy consumption of inter-layer communications.
- **Stress management:** Although diamond has a much lower coefficient of thermal expansion than copper (about 1.2×10^{-6} K^{-1} versus 16.5×10^{-6} K^{-1}), hybrid bonding allows this difference to be managed by means of adaptation layers (e.g., titanium or tungsten) deposited before copper metallisation, as has been demonstrated in material heterogeneity processes.

2.4 Energy and Process Heat: The Thorium Molten Salt Reactor

The fourth pillar of the architecture is the clean, decentralised, high-density energy supply needed to power the industrial production of spherical chips. The fourth-generation thorium molten salt reactor (TMSR) brings together the ideal characteristics for this application.

- **Fuel abundance:** Thorium is approximately three to four times more abundant in the Earth's crust than uranium, and is distributed more homogeneously geographically, reducing dependence on geopolitically concentrated supply chains.
- **Inherent safety:** TMSRs operate at atmospheric pressure (compared to 150 atm for conventional pressurised water reactors), eliminating the risk of explosion due to loss of coolant. In the event of overheating, a frozen salt plug melts by gravity and drains the fuel into passive containment tanks.
- **High operating temperature:** Experimental prototypes, such as the 2 MW TMSR operated by the Chinese Academy of Sciences, reach temperatures above 700 °C, suitable for the cogeneration of electricity and process heat directly in the diamond manufacturing plant.
- **Shorter-lived waste:** Thorium fission generates waste with decay periods of centuries, rather than millennia, and does not produce weapons-usable plutonium, improving non-proliferation.
- **Continuous refuelling:** Salt technology allows fission products to be extracted and new fuel (thorium or uranium-233) to be added without shutting down the reactor, as has already been demonstrated in Chinese prototypes, guaranteeing an uninterrupted energy supply for production lines.

The energy integration is complete: the reactor supplies electricity for CVD equipment, laser sources and control electronics, and process heat (600-700 °C) to maintain the diamond substrates at the required growth temperature and for subsequent annealing of active centres. The TMSR can even directly power the production of hydrogen and methane from atmospheric carbon dioxide through thermochemical cycles, closing the carbon cycle of diamond synthesis.

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3. Applications

The proposed architecture offers decisive competitive advantages in four key areas of classical computing. Each is analysed below.

3.1 Artificial Intelligence and HPC Data Centres

AI and HPC data centres face exponential demand for computing capacity (training models with hundreds of billions of parameters) and a parallel crisis of energy consumption and cooling. Current accelerator chips (GPUs, TPUs, NPUs) reach power densities of 300-500 W per chip and require complex and expensive direct liquid cooling systems.

The application of our architecture to this field offers immediate improvements:

- **Drastic reduction in operating temperature:** Diamond acts as a passive thermal diffuser that transports heat from hot spots to the entire surface of the sphere with a minimal gradient. Preliminary simulations suggest that the maximum junction temperature could be reduced by 30-50 °C compared to a silicon chip of equal power.
- **Higher integration density:** The spherical geometry allows between 8 and 16 active layers of logic and memory circuits to be stacked in a volume of less than 1 cm^3, with ultra-fine-pitch hybrid interconnections offering inter-layer bandwidths of the order of several TB/s.
- **Simplified cooling:** Forced air cooling could be sufficient for many scenarios, eliminating the costly chilled water systems that dominate today's data centres. In extreme configurations, the sphere itself could be immersed in a dielectric fluid in forced circulation, with a uniform heat transfer coefficient thanks to spherical symmetry.

3.2 Power Electronics and Industrial Control Systems

The second application lies in the field of power electronics for systems requiring extreme robustness and efficiency: high-performance electric vehicles,

power converters for smart grids, control systems for harsh industrial environments (steelworks, chemical plants), and space exploration.

Diamond is a semiconductor material with superior properties to silicon carbide (SiC) and gallium nitride (GaN), currently dominant in power electronics. Its extreme bandgap (5.5 eV) and unparalleled thermal conductivity allow it to switch voltages of up to 10 kV and currents of hundreds of amperes with very low switching and conduction losses. Recent market literature estimates that a diamond-based power converter could reduce size and weight by 80 % compared to silicon solutions, and by 60 % compared to SiC.

The spherical architecture, applied to a power module, could integrate into a single sphere of less than 5 mm in diameter: (i) vertical power transistors on the outer layer to maximise heat extraction by convection, (ii) control circuits in intermediate layers, and (iii) integrated transformers and capacitors inside. The absence of bond wires and the reduction of parasitic inductances would improve switching efficiency at frequencies above 1 MHz, where current SiC and GaN modules begin to suffer large losses.

3.3 Embedded Systems for Extreme Environments

The third application concerns computing systems that must operate reliably under extreme temperature, radiation, or pressure conditions: planetary exploration probes, nuclear instrumentation, deep-well drilling equipment, and high-performance avionics.

Diamond chips inherit the environmental tolerance properties of the base material. Recent reviews have highlighted that diamond devices can operate without significant degradation at temperatures of up to 500 °C (compared to 125-150 °C for silicon), withstand doses of ionising radiation that would render any conventional semiconductor useless, and are chemically inert against most corrosive gases.

A spherical diamond chip would house a complete data acquisition, control and communications system in a volume of a few cubic millimetres, with its own integrated power supply. Its mechanical resistance to vibration and shock is much higher than that of a flat silicon chip, as stresses are distributed homogeneously. The thorium reactor, meanwhile, can be located in remote locations (deserts, polar regions, offshore platforms) without the need for abundant cooling water, supplying on-site energy and process heat for the manufacture and maintenance of these systems.

3.4 Radiofrequency (RF) Signal Processing and High-Speed Communications

The fourth application focuses on RF signal processing, where diamond offers the ideal combination of high cutoff frequency (f_t) and high output power. Diamond RF transistors are being actively researched for their ability to operate at frequencies of tens of gigahertz with output powers per unit area much higher than GaN, currently the reference in this field.

A spherical diamond chip could integrate complete satellite communications or very high-speed point-to-point link transceivers in a single passive autonomous element, with its own antenna conformed on the sphere's surface. Spherical symmetry would allow near-isotropic or directional radiation patterns, depending on the design, and diamond's thermal handling capability would prevent power amplifier degradation even at output levels of tens of watts in a confined space.

Table 1 summarises the comparative metrics of the proposed architecture against current solutions in each of the four applications.

Table 1. Quantitative comparison of the proposed architecture versus conventional technologies.

Application	Current Technology	Key Metric	Current Value	Proposed Value	Estimated Improvement
HPC/AI (AI chip)	Silicon GPU (400 W)	Max power density	~200 $W \cdot cm^{-2}$	~50 $W \cdot cm^{-2}$	×4 lower
HPC/AI (AI chip)	Silicon GPU (400 W)	Max junction temperature	85-105 °C	55-75 °C	30-35 °C lower
Power electronics	SiC module 1.2 kV	Power density ($kW \cdot kg^{-1}$)	5-10 $kW \cdot kg^{-1}$	25-40 $kW \cdot kg^{-1}$	×4-5 higher
Power electronics	SiC module 1.2 kV	Operating temperature	200 °C	350-500 °C	×2 to ×2.5 higher
High-power RF	GaN HEMT	Cutoff frequency (f_t)	~100 GHz	~200 GHz	×2 higher

Application	Current Technology	Key Metric	Current Value	Proposed Value	Estimated Improvement
Extreme environments	Silicon + shielding	Radiation dose (kGy)	1-10 kGy	>500 kGy	×50-500 higher

Sources: own elaboration based on data from the references included in the bibliography.

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4. Discussion

4.1 Challenges for Industry, Scalability, Materials, Manufacturing, and Integration

Despite the enormous potential of the architecture, its practical realisation requires overcoming significant challenges affecting five main areas.

Industry and scalability challenges. The semiconductor industry has spent several decades optimising 2D processes on planar silicon wafers up to 300 mm and 450 mm scales. Migrating to spherical substrates would require completely redesigning all manufacturing stations (deposition, etching, lithography, packaging, and testing). The capital cost of a spherical chip production line would be comparable to that of a next-generation semiconductor fab, with estimates between $15 billion and $20 billion. The question is whether the benefits justify this outlay. In the short term, planar diamond substrates, without the additional complexity of spherical geometry, are probably the best option. In the long term, the integration of new patterning techniques would make the sphere viable.

Materials and manufacturing challenges. Despite the notable advances in polycrystalline and monocrystalline diamond obtained by CVD, the growth of thick layers (greater than 50-100 µm) on curved surfaces introduces internal stresses and composition gradients that can cause delamination or cracking. Reports on the manufacture of spherical diamond capsules for inertial confinement fusion have demonstrated the growth of layers of up to a few hundred micrometres on silicon mandrels of a few millimetres in diameter, with subsequent selective removal of the core. Mass production of thousands of spheres per batch would require specially designed CVD reactors with multi-axis rotation systems and precise gas flow control.

Integration and packaging challenges. Connecting a sphere to a traditional motherboard adds additional difficulties. The most practical approach is a socket in the shape of a truncated cone or a contact hemisphere with pogo-pin-type micro-needles distributed in a spherical pattern, which would allow connection passing over dead points and a certain mechanical tolerance during insertion. Optical interconnections — using fibres integrated into the socket — could complement electrical ones for higher-speed and higher-density signals.

Lithography and patterning challenges. Although acoustic patterning for simple structures is well established in laboratory environments, achieving the nanometric precision required for the most advanced transistors has not been demonstrated to date outside of a few very specific studies. The combination of acoustic techniques for macroscopic guidance and optical techniques (two-photon lithography, electron beam writing on the curved surface) for fine details seems the most promising path, but requires considerable further development.

Energy integration challenges. Although thorium MSRs are heralded as the most promising fourth-generation technology, no large-scale commercial plant has yet been deployed. The Chinese experimental TMSR prototype of 2 MW, the only operational facility of its kind in the world, reached the world milestone of demonstrating the conversion of thorium into uranium-233 within the reactor, but it is not connected to the electricity grid. The thorium supply chain — extraction, purification, fluorination, and dissolution in molten salts — must still be industrialised on a large scale. In addition, the management of fission waste (products with half-lives of centuries) requires a geological storage or recycling strategy that is not yet commercially resolved.

4.2 Technological Feasibility: Speculation or Achievable Foresight?

When evaluating the proposal, it is useful to distinguish between components that already exist (as laboratory prototypes) and integration, which is the genuinely novel element and the subject of speculation.

- **Spherical diamond manufactured by CVD:** Prototypes of hollow polycrystalline diamond spheres for inertial confinement fusion exist, with diameters of up to 2 mm and thicknesses of tens of micrometres.
- **High-resolution acoustic lithography:** Techniques such as picosecond ultrasonics achieve a resolution of 100 nm, and acoustic metagratings have been fabricated with three-dimensional patterns using two-photon lithography. Extrapolation to direct patterning of complete circuits has not yet been demonstrated.

- **Cu-Cu hybrid bonding in 3D:** This is a technology at industrial maturity, with interconnection pitches below 10 µm already available and pitches of 5 µm and below under development.
- **Thorium MSR reactor:** There is a single operational experimental prototype in China, with 2 MW of thermal power, and a Danish company (Copenhagen Atomics) plans the production line of container-sized reactors, but large-scale commercialisation has not yet begun.

The synergistic combination of these technologies is therefore viable at the low-scale microelectronic prototype level on a horizon of 10 to 15 years, but the mass industrial production of millions of spherical diamond chips will probably require 20 years or more of focused and applied development.

4.3 Sustainability and Carbon Footprint

A frequently underestimated advantage of the architecture is its potential for a net-negative carbon footprint. Synthetic diamond is formed from carbon obtained from precursor gases such as methane (CH_4). If the methane comes from atmospheric carbon capture through processes such as CO_2 reduction with renewable hydrogen (solar electrolysis), chip manufacturing becomes a highly effective carbon sink. The thorium reactor, by supplying process heat directly, avoids the emissions associated with electricity generation from fossil fuels.

Furthermore, thorium is a by-product of rare earth mining that would otherwise be discarded as low-activity radioactive waste. The TMSR can burn thorium and also recycle actinides from conventional nuclear waste, thus contributing to the circular economy of nuclear fuel.

Finally, the mechanical strength and longevity of diamond chips (estimated lifetimes of decades without significant degradation) could significantly reduce the frequency of replacement and associated electronic waste.

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5. Conclusions

This article has presented and evaluated a radically different architecture for classical high-performance computing, based on the synergistic integration of a multilayer spherical synthetic diamond substrate, hybrid acoustic and optical patterning technologies on curved surfaces, ultra-dense-pitch copper hybrid bonding interconnections, and a fourth-generation thorium molten salt reactor as a source of energy and process heat.

The potential advantages — whose large-scale industrial exploitation will require two or more decades of sustained investment — are as follows:

1. **Unparalleled thermal dissipation:** The thermal conductivity of diamond (2000-2200 $W \cdot m^{-1} \cdot K^{-1}$) eliminates the thermal bottleneck that limits current and future silicon chips.
2. **Higher integration density:** The spherical geometry and hybrid lithography scaling allow the construction of tens of active layers of logic and memory circuits in a single substrate of less than 1 cm in diameter.
3. **Energy sustainability:** The thorium reactor supplies process heat directly to CVD furnaces, with an overall efficiency exceeding 45 %, and enables a net-negative carbon footprint when precursor gases are obtained by atmospheric capture.
4. **Extreme robustness:** Diamond-based devices operate in temperature ranges from -200 °C to +500 °C and withstand radiation doses thousands of times higher than silicon, opening applications in space exploration, nuclear, and harsh industrial environments.

It is hoped that the research community will identify in this proposal a stimulus to explore similar routes of vertical integration of advanced technologies, beyond the incremental optimisation of manufacturing processes on silicon. We pose, as an open question and foresight horizon, whether the spherical diamond chip could become the dominant paradigm for high-performance computing by the middle of the 21st century.

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